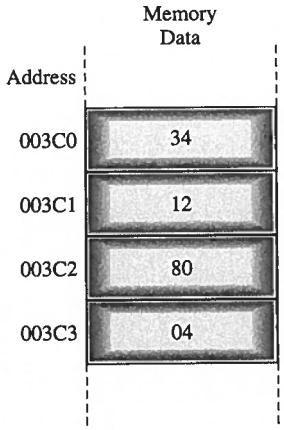
3. How is INTR disabled? How is it enabled?
4. What is the interrupt vector table address for an INT 21H?
5. The address of the ISR for INT 25H is 03C0:9AE2 (in CS:IP format). Show how this address is stored within the interrupt vector table.
6. What is the effective address of the ISR in Question 5?
7. Write the instructions necessary to place the ISR address of Question 5 into its proper place in the interrupt vector table.
8. Show the contents of stack memory after an interrupt has been initiated. Assume that the stack pointer is at address 3C00H prior to the interrupt and that CS, IP, and the flag register contain 0400H, 1890H, and 0182H, respectively.
9. What interrupt number has a vector table address range of 00280H to 00283H?
10. Which interrupt is recognized first, NMI or single-step?
11. Repeat Example 5.2 with an initial AX value of E03FH.
12. What high-priority event might require the use of NMI in a computer designed for aircraft engine control?
13. An analysis of a computer power failure showed that the computer had valid voltage levels for 2.5 milliseconds. Suppose that the microprocessor had an average instruction execution time of 0.2 microseconds. How many instructions can be executed during the power failure?
14. Explain why an orderly software shutdown is possible in Question 13. Assume that the shutdown involves pushing all processor registers onto a stack in NVM.
15. In Example 5.4 what is the highest AL value that will not cause an INTO interrupt?
16. Design an INTR circuit that has only two inputs: $\overline{\text{XINT}}$ and $\overline{\text{YINT}}$. Both signals are active low. $\overline{\text{XINT}}$ should generate interrupt number 90H, and $\overline{\text{YINT}}$, 91H.
17. What are all eight interrupt numbers for the circuit in Figure 5.9?
18. Modify the interrupt circuit of Figure 5.9 so that interrupt numbers 48H through 4FH are produced.
19. If the ONESEC procedure called by NMITIME took more than 18 milliseconds to execute, would any problems arise?
20. What changes must be made to NMITIME if the frequency of the NMI clock is 1800 Hz? We still want to call ONESEC once per second.
21. What is the result of executing INT 20H with AX containing 0303H and BL containing 04? Refer to ISR20H in Section 5.7 for details.
22. Rewrite ISR20H so that four new functions are added. These functions are:

```
AH=05H : NOT AL
AH=10H : AND AL,BL
AH=20H : OR  AL,BL
AH=80H : XOR AL,BL
```

23. Figure 5.12 shows the contents of a few locations within the interrupt vector table. What will the new program counter be when the interrupt that uses these locations is processed?
24. What INT instruction is required in Question 23?
25. How is the single-step interrupt useful for examining the operation of a running program?
26. During an interrupt acknowledge cycle, 30H is placed on the data bus. Where is the ISR address fetched from?
27. The flag register contains 0346H. Will INTO generate an interrupt? Is trace enabled? Are interrupts enabled?

**FIGURE 5.12** For Question 23




28. What do you imagine are some of the problems with these two interrupt service routines:

```
ISR1: PUSH  AX
      PUSH  BX
      ;
      ;body
      ;
      POP  AX
      IRET
```

```
ISR2: PUSH  AX
      PUSH  CX
      ;
      ;body
      ;
      POP  BX
      POP  AX
      RET
```

29. Write an interrupt service routine that will multiply the contents of AX by 7. If the new value of AX is greater than 8400H, call the far routine OVERSCAN. *Note:* OVERSCAN destroys AX, BX, and DI.
30. What instructions are necessary to load a copy of the return address (CS:IP) into registers AX and BX, from *inside* the interrupt service routine? What stack operations may be used?
31. Use DEBUG to execute these three instructions:

```
MOV   DL,41
MOV   AH,2
INT   21
```

What are the results? Remember to use "p" and not "t" to execute INT 21.