Experiment

9

Transistor Base Biasing

PURPOSE AND BACKGROUND

The purpose of this experiment is to verify the voltages and currents in a base-biased circuit as well as to construct its dc load line. In spite of its simplicity, a base-biased circuit does not effectively stabilize a transistor's quiescent point. Consequently, the Q point is affected by the transistor's current gain (β).

Text References 5–1, The DC Operating Point; 5–2, Base Bias.

REQUIRED PARTS AND EQUIPMENT

- ❑ Resistors (¼ W):
  - ❑ 1 kΩ
  - ❑ 560 kΩ
- ❑ 1-MΩ potentiometer
- ❑ Two 2N3904 NPN silicon transistors
- ❑ 0–15 V dc power supply
- ❑ DMM (preferred) or VOM
- ❑ Breadboarding socket
- ❑ Hand-held hairdryer

USEFUL FORMULAS

Quiescent dc base voltage

$$(1) \quad V_B = V_{CC} - I_B R_B = V_{BE}$$

Quiescent dc collector (emitter) current

$$(2) \quad I_C \simeq \frac{V_{CC} - V_{BE}}{R_B/\beta}$$

Quiescent dc base current

$$(3) \quad I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Quiescent dc collector-to-emitter voltage

$$(4) \quad V_{CE} = V_{CC} - I_C R_C$$

dc load line

(5) $I_{C(\mathrm{sat})} \cong \dfrac{V_{CC}}{R_C}$ (saturation)

(6) $V_{CE(\mathrm{off})} = V_{CC}$ (cutoff)

In general, make

(7) $V_{CC} \gg V_{BE}$

PROCEDURE

1. Wire the circuit shown in the schematic diagram in Figure 9–1, and apply power to the breadboard. The pin diagram for the 2N3904 transistor is shown in Figure 9–2.

Measurement of β_{dc}

2. With your multimeter, measure the voltage across the base and collector resistors, and, using Ohm's law, determine the corresponding currents, recording your values in Table 9–1. From these two sets of values, determine the dc current gain or beta (β_{dc}) for this transistor so that

$$\beta_{\mathrm{dc}} = \frac{I_C}{I_B}$$

Record this value of beta in Table 9–1.

3. Use your multimeter to measure individually V_B and V_{CE}. Record your results in Table 9–1.
4. Compare the values of Step 3 with the expected values, using the value of β_{dc} determined in Step 2 and a typical base-emitter voltage of 0.7 V. Record these values in Table 9–1.

Temperature dependency of β_{dc} and operating point

5. Now use a hand-held hair dryer to blow hot air against the transistor's case for a few seconds while measuring the collector current using your multimeter. Does the collector current increase or decrease?

   You should find that the collector current increases, which in turn causes the circuit's Q point to change.

Calculation of saturation and cutoff on dc load line

6. Using Equations 5 and 6 in the "Useful Formulas" section of this experiment, determine the saturation and cutoff points on the dc load line for this circuit, and record these values in Table 9–2. On the blank graph provided, plot the dc load line, using the calculated values of $I_{C(\mathrm{sat})}$ and $V_{CE(\mathrm{off})}$ as the endpoints of the load line. Now plot the Q point based on

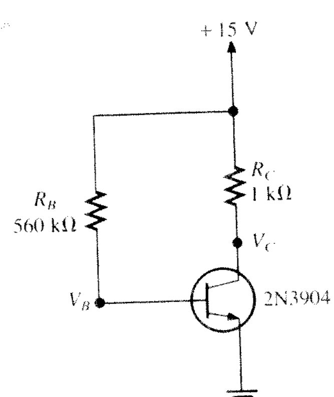


FIGURE 9–1 *Schematic diagram of circuit.*

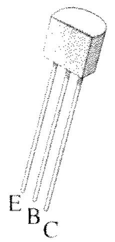


FIGURE 9–2 *2N3904 pin diagram.*

the measured values of I_C and V_{CE} on the same graph. What do you notice about the Q point?

You should find that the measured Q point lies essentially on the dc load line.

7. Using a different 2N3904 transistor, repeat Steps 2 through 5, and record your results in Table 9–1. Do you find any differences between the two transistors?

   You will usually find that the two transistors give different values for the quiescent voltages and currents. In addition, you will usually find differences in the dc current gains.

8. Disconnect the power from the breadboard and replace the 560-kΩ resistor (R_B) with a 1-MΩ potentiometer in series with a 47-kΩ resistor. Again apply power to the breadboard and connect a voltmeter between the transistor's collector terminal and ground.

9. Now vary the resistance of the potentiometer until V_{CE} as read by the voltmeter reaches a maximum value, $V_{CE(\text{off})}$. Then measure the corresponding collector current, $I_{C(\text{off})}$. Record both values in Table 9–2.

10. While continuing to measure the transistor's collector current (I_C), carefully vary the resistance of the 1-MΩ potentiometer until the collector current reaches a *maximum* value. This then is the collector saturation current $I_{C(\text{sat})}$. Now measure the corresponding collector-emitter voltage $V_{CE(\text{sat})}$. Record the values for both $I_{C(\text{sat})}$ and $V_{CE(\text{sat})}$ in Table 9–2.

    At saturation, $V_{CE(\text{sat})}$ is ideally zero, while at cutoff, $I_{C(\text{off})}$ is zero. Plot the values for I_C and V_{CE} at cutoff and saturation on the graph constructed in Step 6. You should find that both points lie essentially on the dc load line very close to the ideal endpoints of cutoff and saturation.

11. Vary the potentiometer so that you are able to measure about five combinations of I_C and V_{CE} over the active region of the dc load line, recording all values in Table 9–2. Then plot these values on the graph. As in Step 10, each point should lie essentially on the dc load line, as the load line is a plot of all possible combinations of I_C and V_{CE}.

FOR FURTHER INVESTIGATION

Try to design a base-biased circuit using a 15-V supply such that the collector-emitter voltage (V_{CE}) is set at approximately 7.5 V.

Name ______________________ Date ______________________

DATA FOR EXPERIMENT 9—TRANSISTOR BASE BIASING

TABLE 9–1
dc values.

Parameter	Transistor 1		Transistor 2	
	Measured Value	Expected Value	Measured Value	Expected Value
I_B				
I_C				
β_{dc}				
V_B		0.7 V (typical)		0.7 V (typical)
V_{CE}				

TABLE 9–2
dc load line.

Condition	Calculated Values		Measured Values	
	I_C	V_{CE}	I_C	V_{CE}
Cutoff (Step 9)				
Saturation (Step 10)				
Active Region (Step 11)				

CALCULATIONS

Instructor Approval ______________________ Date ______________________

Experiment

10

Transistor Emitter Biasing

PURPOSE AND BACKGROUND

The purpose of this experiment is to verify the voltages and currents in an emitter-biased circuit as well as to construct its dc load line. Unlike other biasing schemes, emitter bias uses both a positive and a negative supply voltage. In this manner, the base is approximately at ground while the negative emitter-supply voltage forward biases the base-emitter junction.

Text References 5–1, The DC Operating Point; 5–3, Emitter Bias.

REQUIRED PARTS AND EQUIPMENT

- ❑ Resistors (¼ W):
  - ❑ Two 1 kΩ
  - ❑ 4.7 kΩ
- ❑ Two 2N3904 NPN silicon transistors
- ❑ Two 0–15 V dc power supplies
- ❑ DMM (preferred) or VOM
- ❑ Breadboarding socket
- ❑ Hand-held hairdryer

USEFUL FORMULAS

Quiescent dc emitter voltage

(1) $V_E = |V_{EE}| - V_{BE}$ (assuming $V_B \approx 0$)

Quiescent dc base voltage

(2) $V_B = |V_{EE}| - I_E R_E - V_{BE}$ (ideally equal to zero)

Quiescent dc collector (emitter) current

(3) $I_C \cong \dfrac{|V_{EE}| - V_{BE}}{R_E + (R_B/\beta)}$ ($I_C \cong I_E$ for large β)

Quiescent dc base current

(4) $I_B = \dfrac{V_B}{R_B} \cong \dfrac{|V_{EE}| - V_{BE}}{\beta R_E + R_B}$

Quiescent dc collector-to-emitter voltage

(5) $V_{CE} = V_{CC} - I_C R_C + V_{BE}$

dc load line

$$(6)\quad I_{C(\text{sat})} = \frac{V_{CC} + |V_{EE}|}{R_C + R_E} \quad \text{(saturation)}$$

$$(7)\quad V_{CE(\text{off})} = V_{CC} + |V_{EE}| \quad \text{(cutoff)}$$

In general, make

$$(8)\quad R_E \gg \frac{R_B}{\beta}$$

$$(9)\quad |V_{EE}| \gg V_{BE}$$

PROCEDURE

1. Wire the circuit shown in the schematic diagram in Figure 10–1, and apply power to the breadboard. The pin diagram for the 2N3904 is given in Figure 10–2.

Measure β_{dc}

2. With your multimeter, measure the base, emitter, and collector voltages, with respect to ground, and measure the base and collector currents, recording your values in Table 10–1. From these two sets of values, determine the dc current gain, or beta (β), for this transistor so that

$$\beta_{\text{dc}} = \frac{I_C}{I_B}$$

Record this value of dc beta in Table 10–1.

3. Then measure V_{CE}, and record your results in Table 10–1.
4. Compare these values and those of Steps 2 and 3 with the expected values, using the calculated value of beta determined in Step 2 and a typical base-emitter voltage of 0.7 V. Record these expected values in Table 10–1.

Temperature changes the operating point

5. Now use a hand-held hair dryer to blow hot air against the transistor's case for a few seconds while measuring the emitter current using your multimeter. Does the emitter current increase or decrease?

   You should find that the emitter current increases, which in turn causes the circuit's Q point to change.

Calculation of cutoff and saturation on dc load line

6. Using Equations 6 and 7 in the "Useful Formulas" section of this experiment, determine the saturation and cutoff points on the dc load line for this

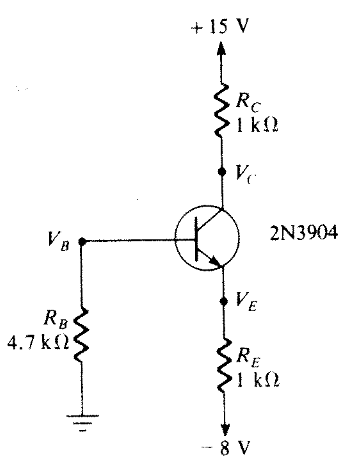


FIGURE 10–1 *Schematic diagram of circuit.*

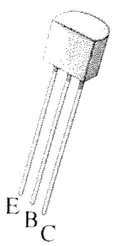
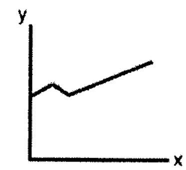


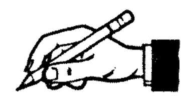
FIGURE 10–2 *2N3904 pin diagram.*

circuit, and record these values in Table 10–2. On the blank graph provided, plot the dc load line, using the calculated values of $I_{C(\mathrm{sat})}$ and $V_{CE(\mathrm{off})}$ as the endpoints of the load line. Now plot the Q point based on the measured values of I_C and V_{CE} on the same graph. What do you notice about the Q point?



You should find that the measured Q point lies essentially on the dc load line.

7. Using a different 2N3904 transistor, repeat Steps 2 through 5, and record your results in Table 10–1. Do you find any differences between the two transistors?



You will usually find that the two transistors give different values for the quiescent voltages and currents. In addition, you will usually find differences in the current gains.

WHAT YOU HAVE DONE

This experiment verified the voltages and currents in an emitter-biased circuit using two power supplies as well as constructed the dc load line for the circuit. In addition, it demonstrated the effect of temperature on the stability of the bias circuit. The data sheet for the 2N3904 translator is given in Appendix B.

Name ______________________ Date ______________________

DATA FOR EXPERIMENT 10—TRANSISTOR EMITTER BIASING

	Transistor 1		Transistor 2	
Parameter	Measured Value	Expected Value	Measured Value	Expected Value
I_C				
I_B				
β_{dc}				
V_B				
V_C				
V_E				
V_{CE}				

TABLE 10–1
dc values.

Parameter	Calculated Value
$V_{CE(off)}$	V
$I_{C(sat)}$	mA

TABLE 10–2
Cutoff and saturation.

CALCULATIONS

Instructor Approval ______________________ Date ______________________