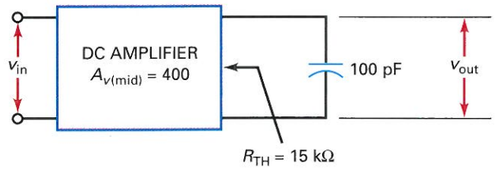
Figure 16-37



SEC. 16-8 THE MILLER EFFECT

16-26 What is the input Miller capacitance in Fig. 16-38 if $C = 5$ pF and $A_v = 200{,}000$?

16-27 Draw the ideal Bode plot for the input lag circuit of Fig. 16-38 with $A_v = 250{,}000$ and $C = 15$ pF.

16-28 If the feedback capacitor of Fig. 16-38 is 50 pF, what is the input Miller capacitance when $A_v = 200{,}000$?

16-29 Draw the ideal Bode plot for Fig. 16-38 with a feedback capacitance of 100 pF and a voltage gain of 150,000.

SEC. 16-9 RISETIME-BANDWIDTH RELATIONSHIP

16-30 An amplifier has the step response shown in Fig. 16-39*a*. What is its upper cutoff frequency?

16-31 What is the bandwidth of an amplifier if the risetime is 0.25 μs?

16-32 The upper cutoff frequency of an amplifier is 100 kHz. If it is square-wave tested, what would the risetime of the amplifier output be?

16-33 In Fig. 16-40, what is the low-cutoff frequency for the base coupling circuit?

Figure 16-38

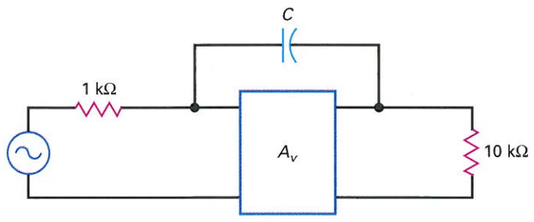


Figure 16-39

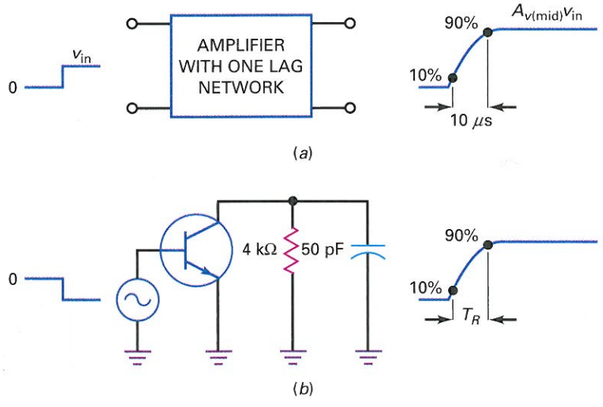
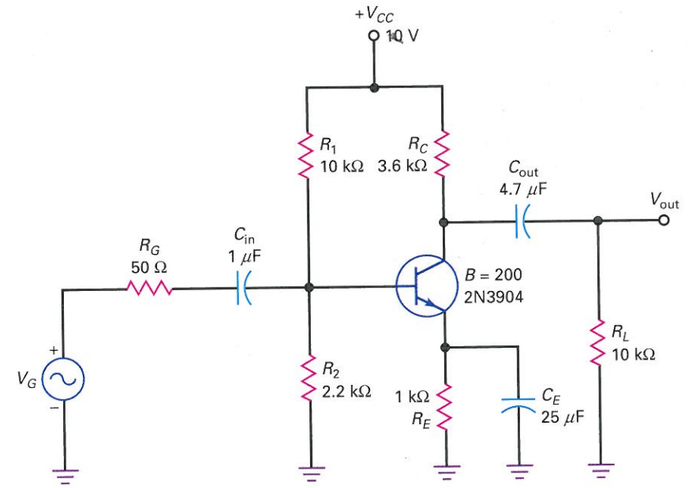


Figure 16-40



16-34 In Fig. 16-40, what is the low-cutoff frequency for the collector coupling circuit?

16-35 In Fig. 16-40, what is the low-cutoff frequency for the emitter bypass circuit?

16-36 In Fig. 16-40, C'_C is given as 2 pF, $C'_e = 10$ pF, and C_{stray} is 5 pF. Determine the high-frequency cutoff values for both base-input and collector-output circuits.

16-37 The circuit of Fig. 16-41 uses an E-MOSFET with these specifications: $g_m = 16.5$ mS, $C_{iss} = 30$ pF, $C_{oss} = 20$ pF, and $C_{rss} = 5.0$ pF. Determine the FET's internal capacitance values for C_{gd}, C_{gs}, and C_{ds}.

16-38 In Fig. 16-41, what is the dominant low-cutoff frequency?

16-39 In Fig. 16-41, determine the high-frequency cutoff values for both gate input and drain output circuits.

Figure 16-41