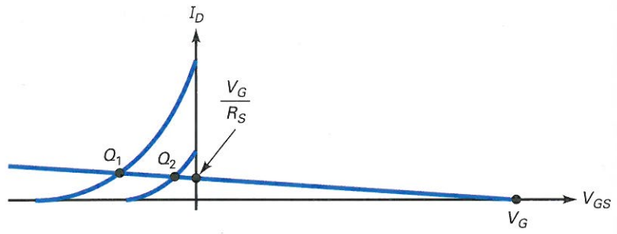
Figure 13-14 VDB Q point.



Example 13-8

Draw the dc load line and the Q point for Fig. 13-15*a* using ideal methods.

SOLUTION The 3:1 voltage divider produces a gate voltage of 10 V. Ideally, the voltage across the source resistor is:

$$V_S = 10 \text{ V}$$

The drain current is:

$$I_D = \frac{10 \text{ V}}{2 \text{ k}\Omega} = 5 \text{ mA}$$

and the drain voltage is:

$$V_D = 30 \text{ V} - (5 \text{ mA})(1 \text{ k}\Omega) = 25 \text{ V}$$

The drain-source voltage is:

$$V_{DS} = 25 \text{ V} - 10 \text{ V} = 15 \text{ V}$$

The dc saturation current is:

$$I_{D(\text{sat})} = \frac{30 \text{ V}}{3 \text{ k}\Omega} = 10 \text{ mA}$$

and the cutoff voltage is:

$$V_{DS(\text{cutoff})} = 30 \text{ V}$$

Figure 13-15 Example.

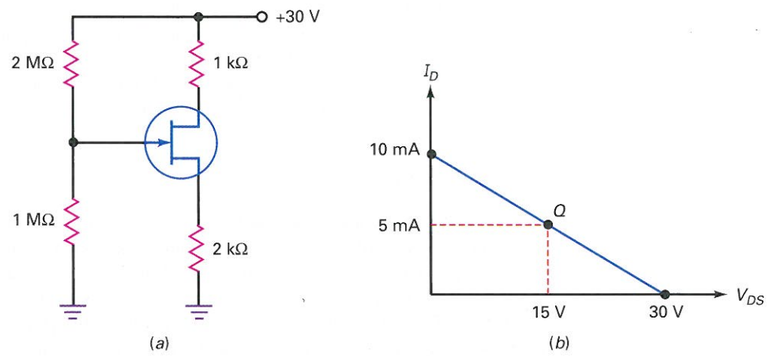


Figure 13-15*b* shows the dc load line and the Q point.

PRACTICE PROBLEM 13-8 In Fig. 13-15, change V_{DD} to 24 V. Solve for I_D and V_{DS} using ideal methods.

Example 13-9

MultiSim

Again using Fig. 13-15*a*, solve for the minimum and maximum Q point values using the graphical method and transconductance curves for a 2N5486 JFET shown in Fig. 13-16*a*. How does this compare to the measured values using MultiSim?

Figure 13-16 (*a*) Transconductance; (*b*) MultiSim measurements.