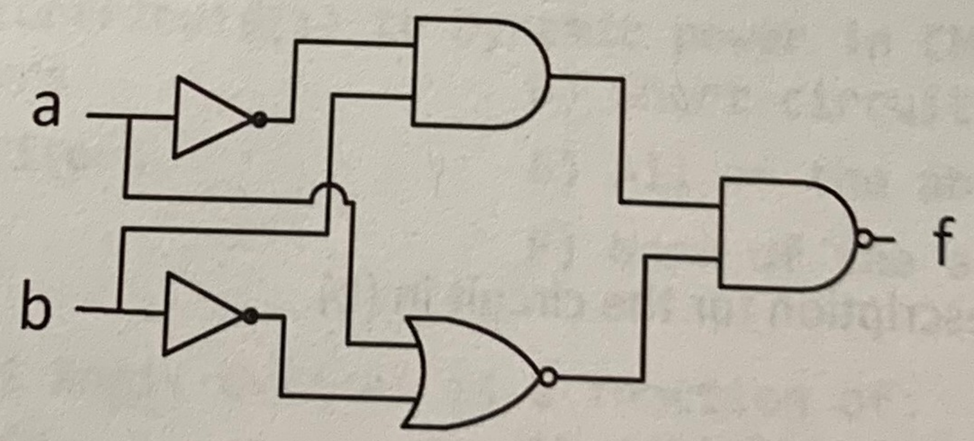
1. (25 pts) A microcontroller can operate over a power supply range of 1.8 V to 5.5 V at clock frequency ranges from 0 to 20 MHz. It dissipates a maximum power of 40 mW. If this microcontroller is operated using a supply voltage of 2.5 V at clock frequency 10 MHz estimate the power consumption for this microcontroller at this operating condition?

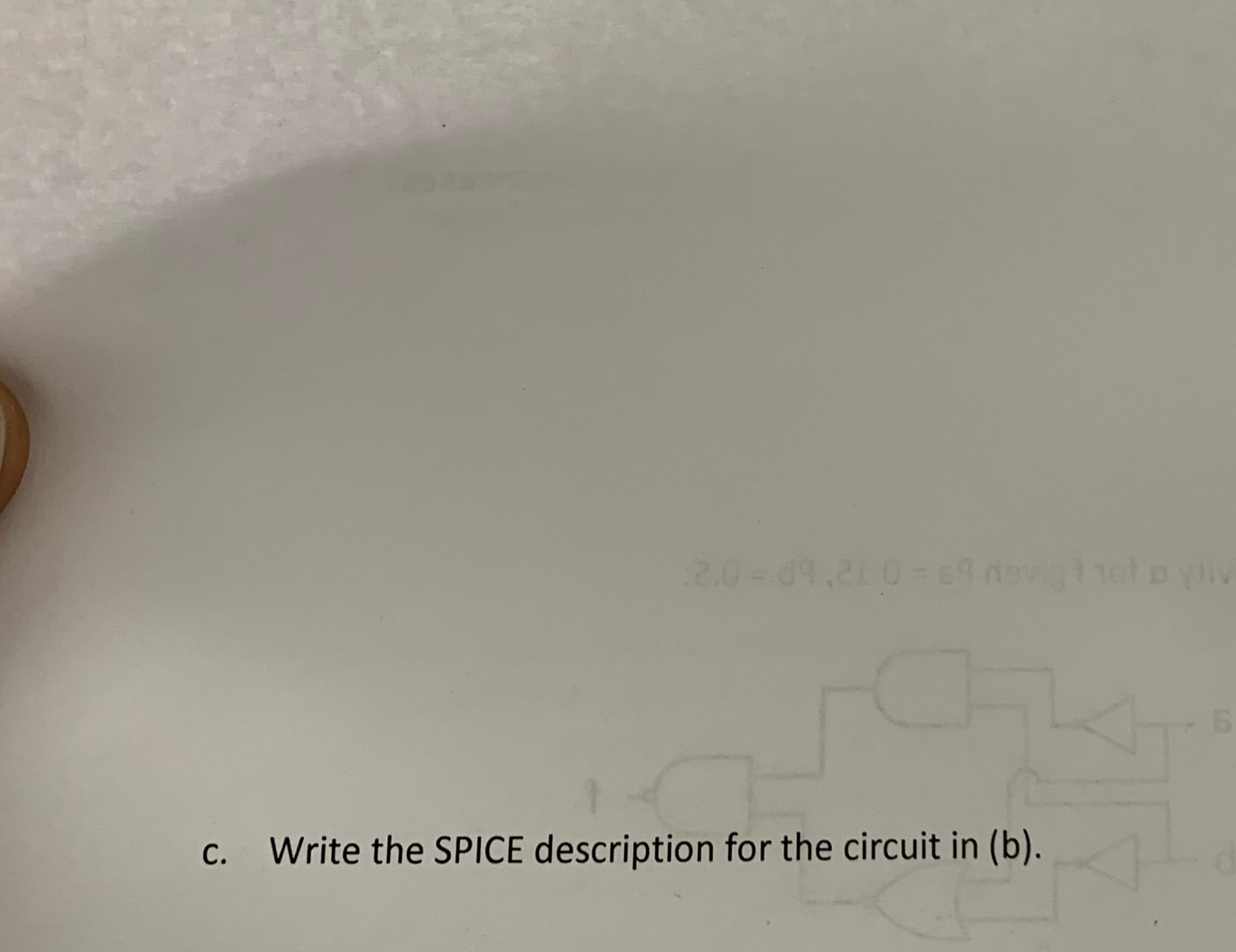
2. *(25 pts)* Calculate the activity α for f given Pa = 0.15, Pb = 0.5:



3. (30 pts) Implement function f(a,b,c) = (a+b)c' using CMOS logic.

a. Write the equation for the PDN:

b. Draw the complete CMOS schematic and indicate the W/L ratio for each transistor such that its output current is equivalent to that of an inverter. The reference inverter W/L for NMOS is 1 and W/L for PMOS is 2. Assume a', b', and c' input signals are available.



c. Write the SPICE description for the circuit in (b).

Multiple-Choice Section (20 pts)

1. Characteristics of the sub-100 nm transistors:
   A) low power but slow
   B) saturate quickly but leaky
   C) fabrication friendly
   D) uniform threshold voltages
   E) All of the above
   F) None of the above

2. The impact of DIBL in sub-100 nm transistors:
   A) increases heat dissipation
   B) decreases heat dissipation
   C) VGD can affect Drain leakage
   D) VDS affects VTH
   E) All of the above
   F) None of the above

3. The impact of GIDL in sub-100 nm transistors:
   A) increases heat dissipation
   B) decreases heat dissipation
   C) Vgd can affect Drain leakage
   D) Vds affects Vth
   E) All of the above
   F) None of the above

4. The behaviors of sub-100 nm transistors when temperature increases:
   A) mobility decreases
   B) On-current decreases
   C) Off-current increases
   D) lower threshold voltage
   E) All of the above
   F) None of the above

5. Short-circuit power in CMOS logic devices is caused by:
   A) PUN and PDN conduct
   B) too low ambient temperature
   C) velocity saturation
   D) sub-micron effects
   E) All of the above
   F) None of the above

6. Which of the below contribute(s) to Dynamic power in CMOS logic devices?
   A) Charging capacitors
   B) Discharging capacitors
   C) Glitches
   D) Short-circuit currents
   E) All of the above
   F) None of the above

7. Dynamic power in CMOS logic devices is a function of:
   A) switching frequency
   B) supply voltage
   C) capacitance
   D) activity factor
   E) All of the above
   F) None of the above

8. Glitching in static CMOS logic devices is caused by:
   A) switching frequency too low
   B) unbalanced input delay paths
   C) too much capacitance
   D) unknown reasons
   E) All of the above
   F) None of the above

9. LCFF is needed when:
   A) signals go from low Vth to high Vth
   B) signals go from high Vth to low Vth
   C) signals go from low Vdd to high Vdd
   D) signals go from high Vdd to low Vdd
   E) All of the above
   F) None of the above

10. Transistor leaks come from?
   A) Diffusion currents
   B) DIBL
   C) GIDL
   D) Gate leakage
   E) All of the above
   F) None of the above