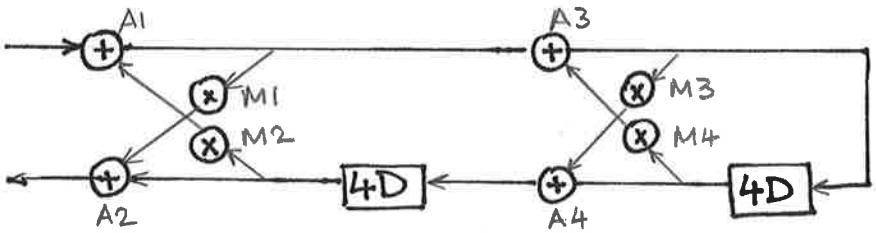
EEE 526: Assignment 2

Due Oct 1, 2021

1. Compute the critical path time of the IIR filter circuit shown below. Assume that addition and multiplication take 1 u.t. and 2 u.t., respectively. Redistribute the delays to achieve a critical path delay of 2 u.t.

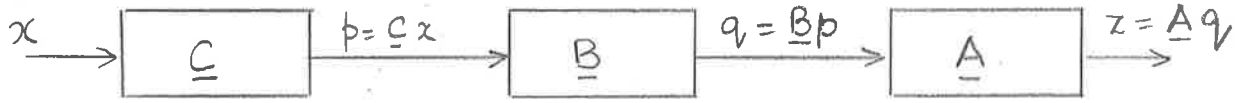


2. Consider the IIR filter with $y(n) = x(n) + ax(n-1) + by(n-2)$. What is the iteration period if the multiplier delay is 10ns and the adder delay is 2ns? Pipeline the filter so that it can be clocked at (i) 6ns, (ii) 3ns.

3. Consider the IIR filter $H(z) = \frac{0.5+0.25z^{-1}}{(1-0.25z^{-1})(1-0.5z^{-1})(1-0.75z^{-1})}$. Pipeline the filter so that each multiply-add can be pipelined to 2 stages. Draw the complete structure with latches in appropriate locations.

4. Consider a first order IIR filter with transfer function $1/(1-az^{-1})$. Implement this filter with a sample period of one-fourth multiply-add time by (i) 4-stage pipelining, and (ii) 4-stage block processing (incremental) with block size of 4. What are the advantages/disadvantages of the two implementations.

5. Design a 3-stage systolic array system which computes $Z = ABCx$ as shown in the figure below. Here A, B and C are $N \times N$ matrices and x is an $N \times 1$ vector. What should be the data flow such that the three stages are I/O matched, i.e. additional buffers are not required between stages?



6. One of the systolic arrays for convolution is given in the figure below. What is the dependence graph, projection vector and schedule vector that would result in this systolic array?

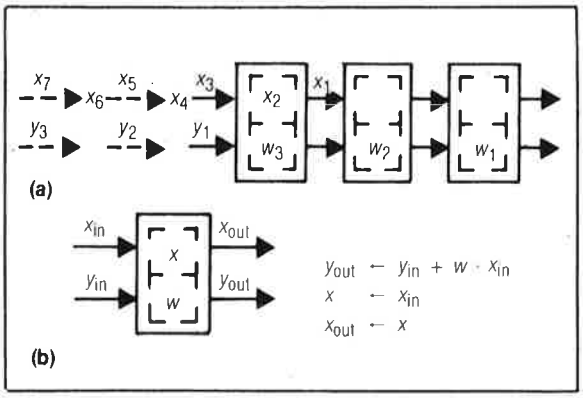


Figure 9. Design W2: systolic convolution array (a) and cell (b) where w_i's stay and x_i's and y_i's both move systolically in the same direction but at different speeds.

Source: H.T. Kung's paper, "Why Systolic Architectures", IEEE Computer, Jan '82