- **See last page for important submission instructions**
- **Due Date: Monday, February 12, 2018 at 10:00:00 P.M. Pacific Daylight Time (PDT)**

Notes:

- *You will find it useful to refer to the OA tutorial from class and the official OA documentation.*
- *Use the skeleton C++ code provided in the Lab 3 materials directory listed above – it is nearly identical to the Lab 1 skeleton. You will likely find it helpful to refer to your own Lab 1 solution as frequently as needed to develop your solution for this lab. We've provided a shell script to import the design into an OA database for your convenience.*
- *You should do Problem 1 first, as Problem 2 relies on it working correctly.*
- *Please use Piazza for asking (and answering) questions before coming to office hours. However, you are expected to work on the assignment alone, so do not provide solutions or compare results with your peers.*

For this assignment, you will develop a partition algorithm and implement it in C++ using the OpenAccess (OA) API.

Problem 1 (2 points): Determine the total wirelength for all nets.

This lab builds on your work from Lab 1, where you computed the half-perimeter wirelength (HPWL) of logic nets in a design. Write a small C++ routine to determine the HPWL for *all* nets in the design, including power, ground, clock, floating, etc. Justify your assumptions as necessary, like you did in Lab 1. For nets with more than two endpoints, use the half perimeter of the smallest bounding box that includes all endpoints. Output the *total* HPWL of the design.

In the report, describe your algorithm for computing total HPWL in words and include the total HPWL for the design.

Problem 2 (8 points): Partition the placement.

Write a C++ routine to partition the instances of the design into two parts, where the partition should be as balanced as possible, and the cut cost should be minimized. The cost of the partition is defined as follows:

1. Balance cost ***B = |(# of gates in partition1) - (# of gates in partition2)| / (total # of gates)***.
2. Cut cost ***C = (total HPWL of cut nets) / (total HPWL of the design)***.

Your goal is to minimize the total cost ***(B + C)*** and runtime**.** In other words, you should efficiently partition the design into two parts with similar gate counts, and the nets being cut should have small total HPWL. A cut net is defined as the net connected to at least one instance from each of the two partitions.

Note that the partition of your design should be physically reasonable, which is different from logically grouping the design. Fig. 1 shows some examples of valid cuts where the black box is the design placement and colored wires are the cuts. Fig. 2 shows examples of invalid cuts. **You are not allowed to modify the design in any way**.

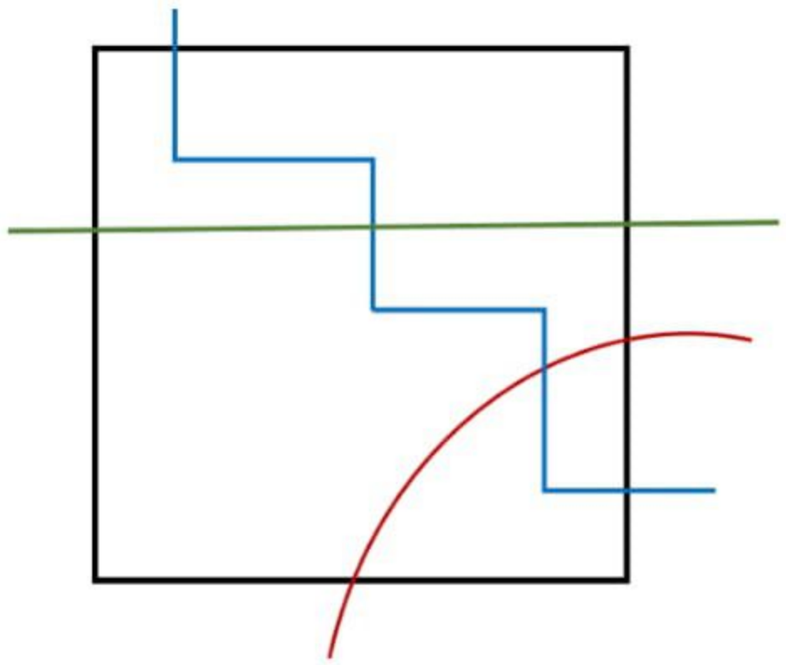

Fig. 1

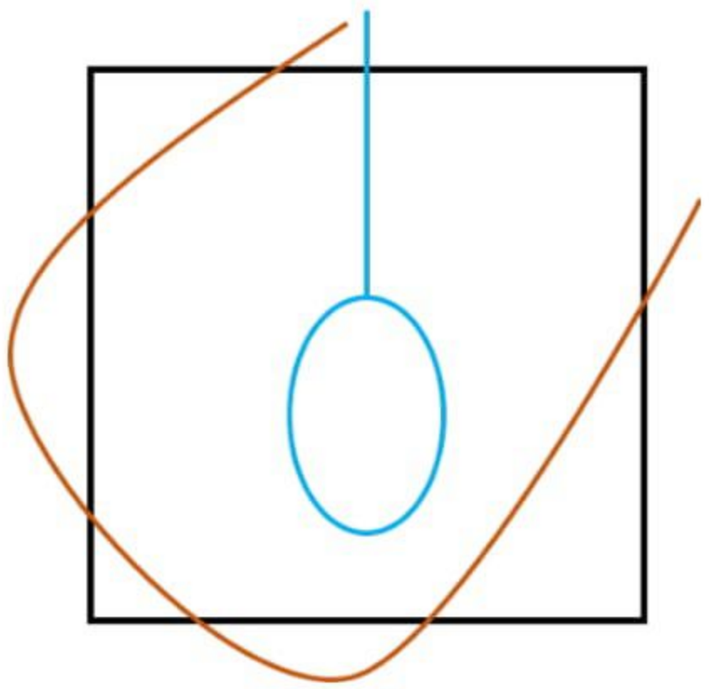

Fig. 2

In the report, describe your approach, give the balance cost ***B***, cut cost ***C***, and the total cost ***(B+C)***. Your program should generate a text file named `Lastname-Firstname_UID_Username_Lab3.result`, which gives instance names of the two partitions, names of the nets being cut and their HPWL separated by comma. The content must follow the ***exact*** format given below otherwise it will not be graded:

```
Partition1:
g8054
g8046
…
Partition2:
g8032
g8031
…
Cut Net:
n_190,3420
n_260,2280
…
```

Grading Notes: 0 point if the partition is not a valid partition or the cut nets listed are not correct according to the partition result. 3 out of the 8 points on Problem 2 will be awarded based loosely on your ranking in the class on the following metric: ***(B + C) + λ*runtime (seconds)***, where ***λ*** will be determined according to the runtime distribution of the whole class, and a lower metric score is better.